

Xilinx Academy III Description:

The Academy III course consists of 3 packaged courses including:

- Advanced FPGA Implementation (2 days)
- Designing with PlanAhead (2 days)
- Debugging Techniques Using Chipscope – Part 2 (1 day)

Attend all 5 days and save! The full Academy is discounted to \$2700 + GST, a saving of \$425 (normal price \$3125 + GST). Attending individual Days are \$625 + GST.

We also offer this course live online with an instructor which is fully interactive and at a further discounted price of \$2295 + GST. Please see www.thelogicportal.com for further details.

A Digilent Demo Board may be purchased with an Academic discount when attending this course. See the end of this brochure for details.

Advanced FPGA Implementation

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE® design suite and Xilinx hardware. Seven labs provide hands-on experience in this two-day training and cover the Xilinx Synthesis Technology (XST) tools.

This course requires the *Essentials of FPGA Design* and *Designing for Performance* courses as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended as is at least six months of design experience with Xilinx tools and FPGAs. The lecture material in this course covers the ISE tools and the Spartan®-6 and Virtex®-6 FPGAs.

Who Should Attend? – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites

- *Essentials of FPGA Design, Designing for Performance*
- Intermediate knowledge of Verilog or VHDL is recommended
- At least six months of Xilinx design experience

Hardware

- Architecture: Spartan-6 and Virtex-6 FPGAs*
- Demo board: Spartan-6 FPGA SP605 board*

After completing this comprehensive training, you will have the necessary skills to:

- Create and edit a User Constraint File (UCF)
- Identify the I/O timing constraints and design modifications required for source-synchronous and system-synchronous interfaces
- Implement designs via the Tcl command line
- Use the PlanAhead™ tool to create area constraints
Use design preservation techniques to simplify design ripple effects
- Change signals of interest in the ChipScope™ Pro tool for board-level debugging using the FPGA Editor

Course Outline

- Introduction
- **Lab 1:** Timing Closure Review
- UCF Editing
- **Lab 2:** UCF Editing
- Advanced I/O Timing
- **Lab 3:** Advanced I/O Timing
- Tcl Scripting
- **Lab 4:** Tcl Scripting/Floorplanning an Effective Layout
- **Lab 5:** Floorplanning
- Design Preservation Techniques
- **Lab 6:** Leveraging Design Preservation for Predictable Results
- FPGA Editor: Viewing and Editing a Routed Design
- **Lab 7:** Advanced FPGA Editor

Lab Descriptions

- **Lab 1:** Timing Closure Review – Use the Constraints Editor to enter timing constraints.
- **Lab 2:** UCF Editing – Write constraints directly into a UCF file to guide the performance results of implementation.
- **Lab 3:** Advanced I/O Timing – Compose timing constraints for source-synchronous and system-synchronous I/O interfaces. Analyze the timing and determine changes to optimize the interface timing.
- **Lab 4:** Tcl Scripting – Write ISE tool control commands in Tcl script files to create a project and implement the design. Explore how the Tcl interface is integrated with the Project Navigator tool.
- **Lab 5:** Floorplanning – Implement a design by using floorplanned constraints to improve the timing results over a design without floorplanning.
- **Lab 6:** Leveraging Design Preservation for Predictable Results – Utilize partitions to preserve timing results from one iteration to the next.
- **Lab 7:** Advanced FPGA Editor – Use the FPGA Editor to view and edit a design. Rapidly locate and swap signals of interest for ChipScope Pro tool cores.

Advanced Design With PlanAhead

Learn to increase design performance and achieve repeatable performance by using the PlanAhead™ software tool. Topics include: synthesis and project tips, design analysis, creating a floorplan, improving performance with area constraints and Pblocks, design debugging with the ChipScope™ Pro tool, and design preservation with partitions.

Note: The hands-on labs provided within this course are identical to the tutorials that are packaged with the PlanAhead tool. This course is supplemented with instructor-led presentations and demonstrations.

Who Should Attend? –Engineers interested in analyzing and driving the physical implementation of their designs to maximize performance and capacity.

Prerequisites

- *Essentials of FPGA Design* or equivalent knowledge of the FPGA architecture and the Xilinx ISE® software flow
- *Essential Design with the PlanAhead Analysis and Design Tool* or equivalent knowledge of the PlanAhead software
- *Designing for Performance* recommended

Hardware

- Architecture: Virtex®-6 FPGA*
- Demo board: None*

After completing this comprehensive training, you will have the necessary skills to:

- Use the most advanced features of the PlanAhead software
- Apply the hierarchical viewer and timing report information to make the best area constraints
- Group the best logic into Pblocks
- Import HDL sources, elaborate, and analyze an RTL netlist
- Implement the design with different implementation strategies
- Analyze design statistics, connectivity, timing, placement, and timing critical paths
- Insert ChipScope Pro tool debug cores
- Floorplan the design to improve performance and preserve successful implementation results
- Make placement constraints for dedicated hardware resources

Course Outline

Day 1

- PlanAhead Software Review
- **Lab 1:** PlanAhead Software Review
- RTL Development and Analysis
- **Lab 2:** RTL Analysis
- Placing Dedicated Resources
- **Lab 3:** Placing Dedicated Resources
- Introduction to Pblocks
- Floorplanning Techniques

Day 2

- Floorplanning Case Studies
- **Lab 4:** Design Analysis and Floorplanning for Performance
- Design Preservation with Partitions
- **Lab 5:** Leveraging Design Preservation for Predictable Results
- Debugging with the ChipScope Pro Tool
- **Lab 6:** Debugging with the ChipScope Tool
- Tcl Scripting in the PlanAhead Software
- **Lab 7:** Tcl Commands
- (Optional): Team Design
- (Optional): Routing Optimization in Virtex-6 Devices

Lab Descriptions

Note: All labs within this course are also available as self-guided tutorials, which are packaged with the PlanAhead tool.

- **Lab 1:** PlanAhead Software Review – Illustrates the steps you take to import source HDL files into the PlanAhead tool and synthesize, implement, and analyze the results. Also introduces the PlanAhead tool environment and views.

- **Lab 2:** RTL Analysis – Provides an overview of the RTL development and analysis environment. You will analyze the RTL logic hierarchy, RTL schematic, RTL resource estimations, RTL power estimations, and run an RTL Design Rule Check (DRC).
- **Lab 3:** Placing Dedicated Resources – Introduces the methods for assigning location constraints to dedicated hardware resources. Demonstrates how to assign dedicated clocking resources, work with multi-function I/O pins, and complete a SSN noise analysis.
- **Lab 4:** Design Analysis and Floorplanning for Performance – Introduces the pre- and post-implementation design analysis features of the PlanAhead software. Provides an introduction to some of the capabilities and benefits of using the PlanAhead tool for designing high-end FPGAs.
- **Lab 5:** Leveraging Design Preservation for Predictable Results – Introduces the use of partitions to maintain successful implementation results.
- **Lab 6:** Debugging with the ChipScope Tool – Provides an introduction to using the PlanAhead tool for debugging designs with the ChipScope Pro tool, cores, and Set Up ChipScope Wizard.
- **Lab 7:** Tcl Commands – Use the Tcl interface in the PlanAhead software.

Debugging Techniques Using the ChipScope Pro Tools

This course requires you have a Spartan-6 SP605 board and the ChipScope software which comes with the logic, embedded and system ISE editions (i.e., just not with webpack)

As FPGA designs become increasingly more complex, designers continue look to reduce design and debug time. The powerful, yet easy-to-use ChipScope™ Pro tool solution helps minimize the amount of time required for verification and debug.

Academy III covers day two of this two-day course (Day 1 is part of Academy II) which will expand on effective ways to debug logic and high-speed designs, to optimize design and core performance to over all decrease your overall design development time.

This training will provide hands-on labs that demonstrate how the ChipScope Pro tools can address advanced verification and debugging challenges.

Who Should Attend? – System and logic designers who want to minimize verification and debug time

Prerequisites

- Basic HDL language concepts
- *Designing with VHDL* or equivalent knowledge of VHDL
- *Designing with Verilog* or equivalent knowledge of Verilog
- *Essentials of FPGA Design*
- Intermediate FPGA skills for
- *Designing for Performance*
- ChipScope Pro Software REL strongly recommended (www.xilinx.com/support/training/rel/chipscopepro-rel.htm)

Software Tools

- Xilinx ISE® Design Suite: 13.1 AND ChipScope Pro 13.1

Hardware

- Architecture: N/A*
- Demo board: Spartan-6 FPGA SP605 board*

After completing this comprehensive training, you will have the necessary skills to:

- Select effective test points in your design
- Optimize design and core performance when ChipScope Pro tool cores are used
- Execute various techniques for collecting data, including file storage, scripting, and building custom triggers

Course Outline

Day 2

- Tips and Tricks
- **Lab 5:** Tips and Tricks
- Time for Timing
- Video Demo – Area Groups for Isolation
- Case Studies
- **Lab 6:** FPGA Editor Support for the ChipScope Pro Tool
- Scripting (Optional)*
- **Lab 7:** VIO Tcl Scripting (Optional)*
- Remote Access (Optional)*
- **Lab 8:** Remote Access (Optional)*

* Documentation and lab files are provided for these labs however they are not performed in class due to the setup and/or time requirements and are generally only applicable to a few people using that flow.

Lab Descriptions

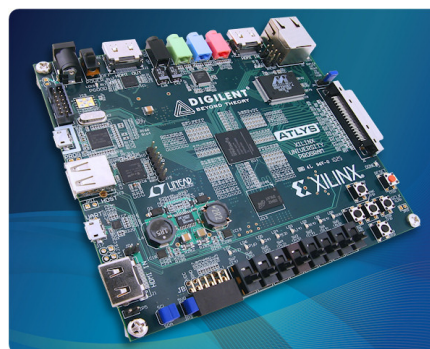
- **Lab 4:** Tips and Tricks – Keep time across multiple sample windows; sample across multiple time domains; and implement a complex custom (unconventional) trigger.
- **Lab 5:** FPGA Editor Support for the ChipScope Pro Tool – Change the signals being sampled by an ILA without having to reimplement the design.
- **Lab 6:** VIO Tcl Scripting – Configure automated analysis.
- **Lab 7:** Remote Access – Use the ChipScope Pro Analyzer tool to configure an FPGA, set up triggering, and view the sampled data

Purchase a Digilent board at Academic pricing when you attend this course.

Please add Tax inside Australia. Pricing correct at time of print, up to date pricing can be found on our online shop.

There are many boards available which can be discounted as part of attending this course. We recommend the following boards. More details on the website.

Spartan-6 Atlys Board



Normal Pricing	AU\$399
Academy Price	AU\$235 - Big Savings!

Spartan-3E Starter Kit



Spartan-3E Starter Kit	500k
Normal Pricing	AU\$210
Academy Price	AU\$189

Register Today

Black Box Consulting delivers public and private courses in locations throughout Australia and New Zealand, and live, instructor led training to attendee's worldwide via a browser based delivery solution, using world class instructors based around the world.

Black Box Consulting is the sole Authorized Xilinx Training Provider for Australia and New Zealand, and is currently the sole authorized live online trainer for Xilinx World Wide

For more information, such as our range of courses, current schedules, and other services including consulting and training packages, please use one of the contact methods below:

Black Box Consulting
PO Box 1147
Stafford City
QLD 4053
Australia

Tel: + 61 7 3137 0905

Fax: +61 7 3 3103 4297

info@blackboxconsulting.com.au

www.blackboxconsulting.com.au

