

For ISE 12.1 release (13.1 release June 2011)

## Xilinx DSP Academy Description:

The 4 day Xilinx DSP Academy course consists of 2 packaged courses including:

- Essential DSP Implementation Techniques for Xilinx FPGAs (2 Days)
- DSP Design using System Generator (2 Days)

**Price: \$2600 + GST for the full 4 day Academy or \$1400 + GST per 2 day course. Xilinx Training Credits accepted at 8 TC's per day.**

## Essential DSP Implementation Techniques for Xilinx FPGAs

This course provides a foundation for Digital Signal Processing (DSP) techniques for Xilinx FPGAs. The course begins with a refresher of basic binary number theory, mathematics, and the essential features within the FPGA that are important to signal processing. The body of the course explores a variety of filter techniques with emphasis on optimal implementation in Xilinx devices and continues with an examination of FFTs, video, and image processing. Throughout the course, Xilinx cores and IP relevant to signal processing are introduced. The course is complemented by hands-on exercises to reinforce the concepts learned.

**Level** – Advanced

**Course Duration** – 2 days

**Who Should Attend?** – Engineers and designers who have an interest in developing products that use digital signal processing

### Prerequisites

A fundamental understanding of digital signal processing theory, including an understanding of the following principles:

- Sample rates
- Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters
- Oscillators and mixers
- Fast Fourier Transform (FFT) algorithm

### Recommended

- *Essentials of FPGA Design* course

After completing this comprehensive training, you will have the necessary skills to:

- Design DSP circuits to utilize the advantages of using FPGAs over traditional processors for DSP designs
- Utilize fixed point binary arithmetic and be able to use this knowledge to create efficient designs in FPGAs
- Design DSP algorithms using the slices in FPGA and the more advanced DSP48 resources
- Identify and evaluate dataflow through the device and use distributed memory, block RAM, registers, and SRLs to properly implement DSP designs
- Analyze different FIR filter and FFT implementations and optimize these implementations in the FPGA
- Evaluate video and imaging systems algorithms, and their implementations in FPGAs

## Course Specification

### Course Outline

#### Day 1

- Agenda
- Back to Basics
- Architecture
- FPGA Math
- **Exercise 1:** Signed Number Conversion, Quantization and Rounding, Adders, Subtractors, and Accumulation
- Shift Registers, RAM, and Applications
- **Exercise 2:** SRL32E and RAM Estimation and Concatenation
- FIR Filter
- **Exercise 3:** Filter Implementation, Resource and Performance Estimation

#### Day 2

- Advanced Filter Techniques
- **Exercise 4:** Filter Implementations, Resource and Performance Estimation
- Fast Fourier Transform
- **Exercise 5:** FFT Implementation, Resource and Performance Estimation
- Video and Imaging
- Where Do We Go From Here?
- **Demonstration:** System Generator and the CORE Generator Tool with a DSP-Targeted Reference Design
- Where Can I Learn More?

### Lab Descriptions

- **Exercise 1:** Signed Number Conversion, Quantization and Rounding, Adders, Subtractors, and Accumulation – Learn how to estimate device resource utilization for basic math functions. Compare different methodologies for implementing functions.
- **Exercise 2:** SRL32E and RAM Estimation and Concatenation – Learn how to optimize memory and storage in Xilinx FPGAs.
- **Exercise 3:** Filter Implementation, Resource and Performance Estimation – Learn how and when to use various implementation strategies for optimal filter implementation.
- **Exercise 4:** Filter Implementations, Resource and Performance Estimation – Advanced filter topologies are studied. Architect multichannel and multirate filters using various methods. Implementation strategies will be discussed and optimal methods used.
- **Exercise 5:** FFT Implementation, Resource and Performance Estimation – Select correct parameters for FFT implementations to meet design targets. Resource estimation will be studied and trade-offs with performance examined through implementation examples.
- **Demonstration:** System Generator and the CORE Generator Tool with a DSP-Targeted Reference Design — Introduces DSP-targeted hardware boards and software tools. Witness the power, ease of use, and design efficiency of Xilinx DSP tools and IP. Reinforce the concepts studied in the course material and exercises.

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## DSP Design Using System Generator

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware co-simulation verification. Through

### Level – Advanced

**Who Should Attend?** – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design

### Prerequisites

- Experience with the MATLAB and Simulink software
- Basic understanding of sampling theory

### Software Tools

- Xilinx ISE® Design Suite: System Edition 12.1
- MATLAB with Simulink software R2009b

### Hardware

- Architecture: Spartan®-6 and Virtex®-6 FPGAs\*
- Demo board: Spartan-6 FPGA SP605 board

hands-on exercises, you will implement a design from algorithm concept to hardware verification using the Xilinx FPGA capabilities.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Use custom boards for hardware co-simulation
- Identify the high-level blocks available for FIR and FFT designs
- Design a multiple-clock-based System Generator system
- Embed two System Generator designs into a larger design

## Course Outline

### Day 1

- Introduction to System Generator
- Simulink Software Basics
- **Lab 1:** Using the Simulink Software
- Basic Xilinx Design Capture
- **Lab 2:** Getting Started with Xilinx System Generator
- Signal Routing
- **Lab 3:** Signal Routing
- Implementing System Control
- **Lab 4:** Implementing System Control

### Day 2

- Multi-Rate Systems
- **Lab 5:** Designing a MAC-Based FIR Filter Design
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block
- System Generator, Project Navigator, and Platform Studio Integration
- **Lab 7:** System Generator and Project Navigator Integration

## Course Specification

- Spartan-6 and Virtex-6 FPGA DSP Platforms
- **Lab 8:** Using System Generator to Develop Virtex-6 and Spartan-6 FPGA DSP Applications

## Lab Descriptions

- **Lab 1:** Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.
- **Lab 2:** Getting Started with Xilinx System Generator – Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.
- **Lab 3:** Signal Routing – Design padding and unpadding logic by using signal routing blocks.
- **Lab 4:** Implementing System Control – Design an address generator circuit by using blocks and Mcode.
- **Lab 5:** Designing a MAC-Based FIR – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using a Xilinx demo board.
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block – Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 7:** System Generator and Project Navigator Integration – Learn how to embed two System Generator designs into a larger design and how VHDL created by System Generator can be incorporated into the simulation model of the overall system.
- **Lab 8:** Using System Generator to Develop Virtex-6 and Spartan-6 FPGA DSP Applications – Design a single-carrier Digital Up Converter (DUC) and Digital Down Converter (DDC) to meet WCDMA UTMS 3GPP specifications.

## Register Today

Black Box Consulting delivers public and private courses in locations throughout Australia and New Zealand, and live, instructor led training to attendee's worldwide via a browser based delivery solution

For more information, such as our range of courses, current schedules, and other services including consulting and recruitment/training packages, please use one of the contact methods below:

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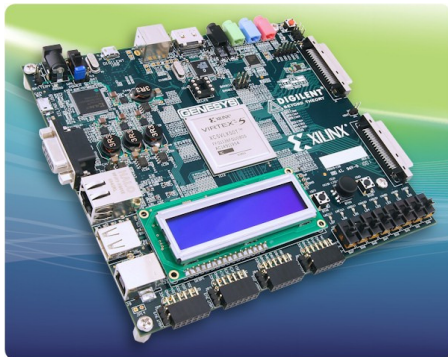
## Qualify for Academic Pricing for the below boards when you attend the DSP Academy

(Please add GST inside AU)

### XUPV5 OpenSPARC Eval - Board



### Digilent Genesys Virtex-5 Eval - Board



	XUPV5 OpenSPARC	Genesys Virtex-5
Normal Pricing	\$2400	\$1295
Academic Price	<b>\$975!!</b>	<b>\$600!!</b>

## Training



Xilinx education courses are conducted throughout Australia and New Zealand and are presented by Xilinx FPGA experts.

Live, instructor led online courses can be presented throughout the world.

## Design Support Consulting



Have a Xilinx expert working on your FPGA project along side your team either onsite or remotely. Short term assistance available via our remote assistance and training technology

## Recruitment



Black Box Consulting has 6 years recruiting experience from Engineering roles through to Sales and General Managers. Experience professional recruitment services which manage the complete process, not just CV flicking!

## Digilent Reseller



Black Box Consulting distributes Digilent FPGA and Microcontroller evaluation boards, which have reductions for course attendees and students.



We also distribute over 35 different peripheral boards from RS232, Ethernet, Audio, LEDs, LCDs, switches, ADCs and DACs to drivers, connection adapters and breadboards.



We also ship USB, Parallel, JTAG and Xilinx iMPACT cables at a much cheaper rate than you will find elsewhere.