Fundamentals of CPLD Design

CPLD13000-9-ILT (v1.0)

Course Specification

Course Description

This comprehensive course provides you with an introduction to designing with Xilinx CPLDs by using the ISE™ series software tools. You will learn the basics of ISE software flow and how to interpret CPLD reports for optimum performance designs.

This course covers ISE features such as the Constraints Editor and PACE. Other topics include design planning, implementation options, and global timing constraints. You will ultimately configure a CPLD demo board by using Xilinx configuration software.

Level – Fundamental
Course Duration – 1 day
Price – AU$550 + GST (both CPLD Courses $900 + GST) Online only
Course Part Number – CPLD13000-9-ILT
Who Should Attend? – Digital designers who have working knowledge of basic HDL (VHDL or Verilog) and who are new to Xilinx CPLDs, ISE software, or both
Prerequisites
- Basic HDL knowledge (VHDL or Verilog)
- Digital design experience

Software Tools
- Xilinx ISE 9.1i

Recommended Hardware Demo Board

After completing this comprehensive training, you will have the necessary skills to:
- Describe what products Xilinx offers and where the CoolRunner-II CPLD fits into this offering
- Identify the basic architectural resources of the CoolRunner-II CPLD
- Describe the CPLD tool flow: Design entry, synthesis, implementation, and programming
- Specify global timing constraints and pin assignments
- Access and implement basic and advanced CPLD software options via the ISE software

Course Outline

- Course Agenda
- Introduction to Xilinx Products
- CoolRunner-II CPLD Architecture
- CPLD Software Flow
- **Lab 1:** Xilinx CPLD Tool Flow
- Reading CPLD Reports
- Global Constraints
- **Lab 2:** Constraints for CPLDs
- CPLD Software Options
- **Lab 3:** CPLD Implementation Options

Lab Descriptions

- **Lab 1:** Xilinx CPLD Tool Flow – Create a new project in the Project Navigator of the ISE software. Implement a design by using default software options and configure the CoolRunner-II CPLD demo board with iMPACT, the Xilinx In-System Programming (ISP) software.

- **Lab 2:** Constraints for CPLDs – Use constraints to specify clock frequencies, pin locations, and I/O standards for the CPLD demo board project. Fit the design and analyze the Timing and Fitter Reports to confirm performance and I/O placement.

- **Lab 3:** CPLD Implementation Options – Implement the design with default software options and evaluate the design performance versus design requirements. Apply a global timing constraint for PERIOD to the design. Change the software options and add I/O constraints to meet the design's timing goals.

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