

Course Description

Learn to increase design performance and achieve repeatable results by using the PlanAhead™ software tool. Topics include: a product overview, synthesis and project tips, design analysis, creating a floorplan, improving performance, experimenting with implementation options, incremental methodology, block-based IP design, and I/O pin assignment.

Note: The hands-on labs provided within this course are identical to the tutorials that are packaged with the PlanAhead software. This course is supplemented with instructor-led presentations and demos.

Level – Intermediate

Course Duration – 2 days

Price – AU\$1400 + GST (\$1200 Early Birds) or 14 Training Credits

Course Part Number – FPGA11000-9-ILT

Who Should Attend? – FPGA designers, system architects, and system engineers who are interested in analyzing and driving the physical implementation of their designs to maximize performance and capacity.

Prerequisites

- *Fundamentals of FPGA Design* or equivalent knowledge of the FPGA architecture and the Xilinx ISE™ software flow
- *Designing for Performance* recommended

Software Tools

- Xilinx ISE 9.1i
- PlanAhead 9.1.2

After completing this comprehensive training, you will have the necessary skills to:

- Import designs into the PlanAhead software project environment
- Analyze design statistics, connectivity, timing, and placement results
- Run the Design Rule Checker (DRC) and Weighted Average Simultaneous Switching Output (WASSO) analysis
- Partition and floorplan designs
- Run ExploreAhead to try multiple implementation strategies
- Import and analyze the implementation results to improve the floorplan
- Floorplan to improve performance and consistency
- Use block-based design and create and reuse module-level IP
- Use PinAhead to import, define and assign I/O pins for the design

Course Outline

Day 1

- Course Overview
- **Lab 1:** Getting Started with PlanAhead
- Design Analysis and Exploration
- **Lab 2:** Design Analysis and Exploration
- Design Partitioning and Top-Level Floorplanning
- **Lab 3:** Design Partitioning and Top-Level Floorplanning
- Implementing a Floorplanned Design
- **Lab 4:** Implementation

Day 2

- Floorplanning Techniques
- **Lab 5:** Floorplanning
- Tuning a Floorplan for Performance
- **Lab 6:** Floorplan Tuning
- Block-Based Design and IP Reuse
- **Lab 7:** Block-Based Design and IP Reuse

Course Specification

- I/O Pin Assignment
- **Lab 8:** I/O Pin Assignment
- Floorplanning Strategies
- Course Summary

Lab Descriptions

Note: All labs within this course are also available as self-guided tutorials, which are packaged with the PlanAhead software.

- **Lab 1:** Getting Started with PlanAhead – Illustrates the steps you take to import a synthesized design into the PlanAhead software so that you can begin floorplanning. Also introduces the PlanAhead software environment and views.
- **Lab 2:** Design Analysis and Exploration – Introduces the analysis features of the PlanAhead software that enable early detection of potential design issues, alternate device selection, initial floorplanning direction, and post-implementation exploration.
- **Lab 3:** Design Partitioning and Top-Level Floorplanning – Introduces the concept of floorplanning. By using automated partitioning tools, you will create a top-level floorplan and experiment with sizing and shaping Pblocks based on resources assigned to them.
- **Lab 4:** Implementation – Introduces the integration of the ISE software implementation tools with the PlanAhead software. Also introduces the ExploreAhead tool for queuing multiple ISE software runs with varying strategies.
- **Lab 5:** Floorplanning – Describes how to analyze implementation results and to use that information to generate a floorplan aimed at increasing design performance.
- **Lab 6:** Floorplan Tuning – Introduces techniques to help close on timing targets consistently.
- **Lab 7:** Block-Based Design and IP Reuse – Describes the steps to implement a block-based methodology that includes the creation and reuse of an IP module.
- **Lab 8:** I/O Pin Assignment – Introduces the PinAhead environment for performing I/O pin assignment

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Black Box Consulting
PO Box 1147
Stafford City
QLD 4053

Tel: + 61 7 3137 0905
Fax: +61 7 3311 5240

www.blackboxconsulting.com.au