

Course Description

Attending the *Designing a LogiCORE PCI Express System* will provide you a working knowledge of how to implement a Xilinx PCI Express® core in your applications. This course focuses on the implementation of a Xilinx PCI Express system within the Connectivity Targeted Reference Design (TRD). With this experience, you can improve your time to market with your PCIe core design. Various Xilinx PCI Express core products will be enumerated to aid you in selecting the proper solution. This course focuses on the AXI streaming interconnect.

Price – AU\$1190 or 14 TCs

Who Should Attend?

- Hardware designers who want to create applications using Xilinx IP cores for PCI Express
- Software engineers who want to understand the deeper workings of the Xilinx LogiCORE™ PCI Express solution
- System architects leveraging key Xilinx advantages related to performance, latency, and bandwidth in PCIe applications

Prerequisites

- Experience with PCIe specification protocol
- Knowledge of VHDL or Verilog
- Some experience with Xilinx implementation tools
- Some experience with a simulation tool, preferably ISim
- Moderate digital design experience

Software Tools

- Xilinx ISE® Design Suite: Logic or System Edition 13.1
- ChipScope™ Pro software 13.1

Hardware

- Architecture: Spartan®-6 and Virtex®-6 FPGAs
- Demo board: Spartan-6 FPGA SP605 or Virtex-6 FPGA ML605

After completing this comprehensive training, you will have the necessary skills to:

- Construct a basic PCIe system by:
 - Selecting the appropriate core for your application
 - Specifying requirements of an endpoint application
 - Connecting this endpoint with the core
 - Utilizing FPGA resources to support the core
 - Simulating the design
- Identify the advanced capabilities of the PCIe specification protocol and feature set

Course Outline

Day 1

- Course Introduction
- Introduction to the PCIe Architecture
- Review of the PCIe Protocol
- PCIe and the CORE Generator™ Interface
- **Lab 1:** Constructing the PCIe Core
- Simulating a PCIe System Design
- Connecting Logic to the Core – AXI Interface
- Packet Formatting Details
- **Lab 2:** Downstream Port Model Simulation

Day 2

- Endpoint Application Considerations
- **Lab 3:** Pseudo-Transactional Modeling
- Application Focus: DMA
- **Lab 4:** Design Implementation

- Virtex-6 FPGA Root Port
- Compliance and Debugging
- **Lab 5:** Debugging the PCIe Core with the ChipScope Pro Tools
- Errors and Interrupts
- Course Summary
- Appendix: Mechanicals, Hot Plug, and Power
- Appendix: Connecting Logic to the Core – Local Link

Lab Descriptions

- **Lab 1:** Constructing the PCIe Core – This lab familiarizes you with all the necessary flow of the Xilinx CORE Generator™ tool for generating a Xilinx LogiCORE Endpoint Block IP. You will select appropriate parameters for the CORE Generator tool and create the PCIe core used throughout the labs.
- **Lab 2:** Downstream Port Model Simulation – This lab demonstrates how timing and behavior of a typical link negotiation using the ISim tool. You will observe and capture the effects of link training and write packets to the endpoint application for later use.
- **Lab 3:** Pseudo-Transactional Modeling – This lab illustrates pseudo-transactional modeling, which provides various packets to the user design without the need to simulate the PCIe cores themselves.
- **Lab 4:** Design Implementation – This lab familiarizes you with all the necessary steps and recommended settings to turn the HDL source to a bitstream.
- **Lab 5:** Debugging the PCIe Core with the ChipScope Pro Tools – This lab illustrates how to use the ChipScope™ Pro tools to monitor the behavior of the core and the endpoint application for proper operation.

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Black Box Consulting. PO Box 1147. Stafford City, QLD 4053
Tel: + 61 7 3137 0905 Fax: +61 7 3 3103 4297
info@blackboxconsulting.com.au www.blackboxconsulting.com.au

