

Course Description

This course will appeal to engineers who have an interest in developing low cost products particularly in high volume markets. The course and exercises cover several different design techniques, which will be interesting and challenging for any digital designer regardless of the final application.

Level – Fundamental / Intermediate

Course Duration – 1 day

Price -AU \$700 + GST (\$600 Early Birds) or 7 Training Credits

Who Should Attend? – Engineers wanting to develop low cost products, particularly in high volume markets, and product designers who need to accurately estimate the size of devices required to implement products to predict costs without requiring the actual design to be implemented

Prerequisites

- An understanding of digital logic design and the concept of an FPGA
- An appreciation of VHDL and CAE design flows is beneficial, but not vital

Supported Devices

Note: No software is needed to run this workshop.

- Spartan[™]-3
- Spartan[™]-II(E)

After completing this comprehensive training, you will have the necessary skills to:

- Describe the features of the Spartan-II(E) and Spartan-3 devices
- Accurately estimate design size to aid in predicting product costs
- Apply design techniques that result in low-cost implementations
- Explore creative ways to use the FPGA memory resources to reduce design costs

Course Outline

- What is an FPGA?
- Spartan Family
- CLBs, Slices and BRAM
- Multiplexers
- Flip-Flop Controls
- Synchronous Timing vs. Asynchronous Timing
- Digital Clock Managers
- Dedicated Carry Logic
- Counters
- Wired Carry Gates
- Block Memory
- Distributed RAM
- FIFO
- Dual Port Memory
- PicoBlaze[™] Micro Controller Processor
- State Machines
- Design Challenges

Exercises

- **Exercise 1:** Exploring the Slice
- **Exercise 2:** Logic Levels
- **Exercise 3:** Dedicated Multiplexers
- **Exercise 4:** Performance by Design
- **Exercise 5:** Clocks
- **Exercise 6:** Counters
- **Exercise 7:** Aspect Ratios
- **Exercise 8:** Replacing Logic with Block RAM
- **Exercise 9:** Distributed RAM
- **Exercise 10:** Essence of FIFO
- **Exercise 11:** Delay
- **Exercise 12:** PicoBlaze Microprocessor
- **Exercise 13:** State Machines
- **Design Challenges**
 - Rotational Trigger
 - Operation Clock
 - LED Wall Display
 - Electronic Keyboard

Register Today

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