

## Course Description

*Advanced FPGA Implementation* tackles the most sophisticated aspects of the ISE™ 9.1i tool suite and Xilinx hardware. Seven labs provide hands-on experience in this two-day course and cover Synplicity's Synplify and the Xilinx XST tools. This course requires the *Fundamentals of FPGA Design* and *Designing for Performance* courses as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended as is at least six months' design experience with Xilinx tools and FPGAs. The lecture material in this course covers the ISE software 9.1i tools and the Virtex™-4 FPGAs.

**Level** – Advanced

**Course Duration** – 2 days

**Price** – AU\$1400 + GST (\$1200 Early Birds) or 14 Training Credits

**Course Part Number** – FPGA33000-9-ILT

**Who Should Attend?** – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

### Prerequisites

- *Fundamentals of FPGA Design*
- *Designing for Performance*
- Intermediate knowledge of Verilog or VHDL is strongly recommended
- At least six months' design experience with Xilinx tools and FPGAs

### Software Tools

- Xilinx ISE 9.1i
- Synplicity Synplify Pro 8.8
- Precision 2006.a

After completing this comprehensive training, you will have the necessary skills to:

- Create and edit timing constraints in the UCF file
- Utilize Tcl-based scripting to implement a design
- Analyze I/O interface timing and implement timing constraints and design modifications to meet System and Source Synchronous I/O interface timing
- Utilize Partitions and SmartGuide™ technology to preserve timing results
- Demonstrate floorplanning techniques to enhance timing
- Optimize the post-place-and-route design in the FPGA Editor for more efficient in-circuit testing

## Course Outline

- Introduction
- **Lab 1:** Achieving Timing Closure
- Section 1: Advanced Implementation Control
- Tcl Scripting
- **Lab 2:** Tcl Scripting
- UCF Editing
- **Lab 3:** UCF
- Advanced I/O Timing
- **Lab 4:** Advanced I/O Timing
- Section 2: Design Preservation
- SmartCompile Design Preservation Techniques
- **Lab 5:** SmartCompile
- Floorplanning Effective Layout

- **Lab 6:** Floorplanning
- Section 3: Reduce Debug Time
- FPGA Editor: Viewing and Editing a Routed Design
- **Lab 7:** FPGA Editor

## Lab Descriptions

**Note:** Labs will be based on Xilinx ISE 9.1i software.

- **Lab 1:** Achieving Timing Closure – Create global timing constraints, read timing reports, apply path-specific constraints (multicycle and false paths), and apply advanced implementation options.
- **Lab 2:** Tcl Scripting – Write program commands in a Tcl script file to implement the design. Then modify program switches to obtain the greatest possible performance from the design.
- **Lab 3:** UCF – Write constraints directly into a UCF file to guide the performance results of implementation.
- **Lab 4:** Advanced I/O Timing – Compose timing constraints for I/O interface. Analyze the timing failures and determine changes to correct the timing issues. Modify the design to fix timing failures.
- **Lab 5:** SmartCompile – Utilize SmartGuide and Partitions to preserve timing results from one iteration to the next.
- **Lab 6:** Floorplanning – Implement a design using floorplanned constraints to enhance the timing results over a design without floorplanning.
- **Lab 7:** FPGA Editor – Use the FPGA Editor to view and edit a design. Analyze the contents of a CLB; add a probe; remove, place, and modify components; and analyze long nets.

## Register Today

Black Box Consulting delivers public and private courses in locations throughout Australia and New Zealand.

For more information, such as our range of courses, current schedules, and other services including consulting and recruitment/training packages, please use one of the contact methods below:

Black Box Consulting  
PO Box 1147  
Stafford City  
QLD 4053

Tel: + 61 7 3137 0905  
Fax: +61 7 3311 5240

[www.blackboxconsulting.com.au](http://www.blackboxconsulting.com.au)